

Fig. 1

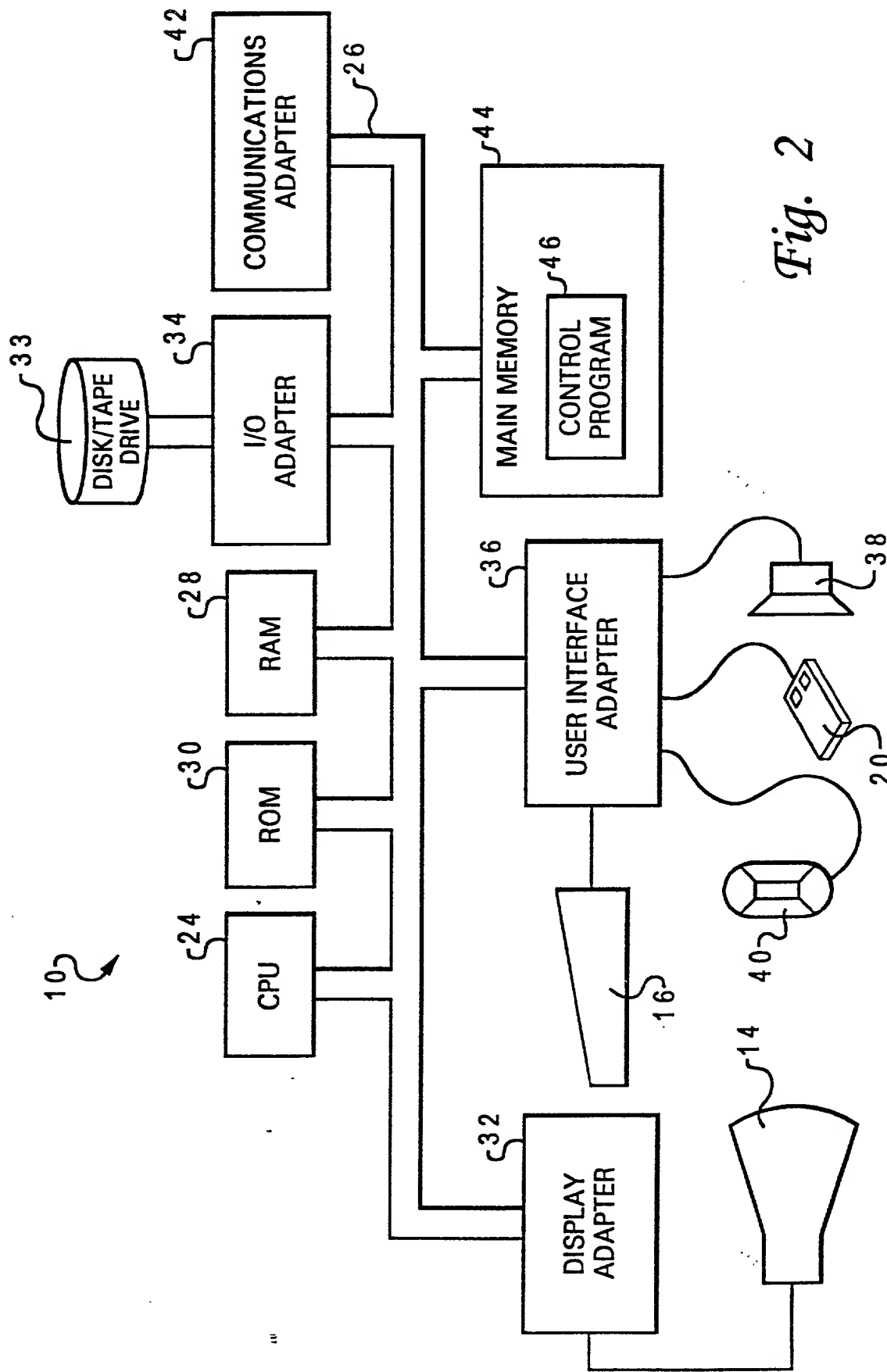


Fig. 2

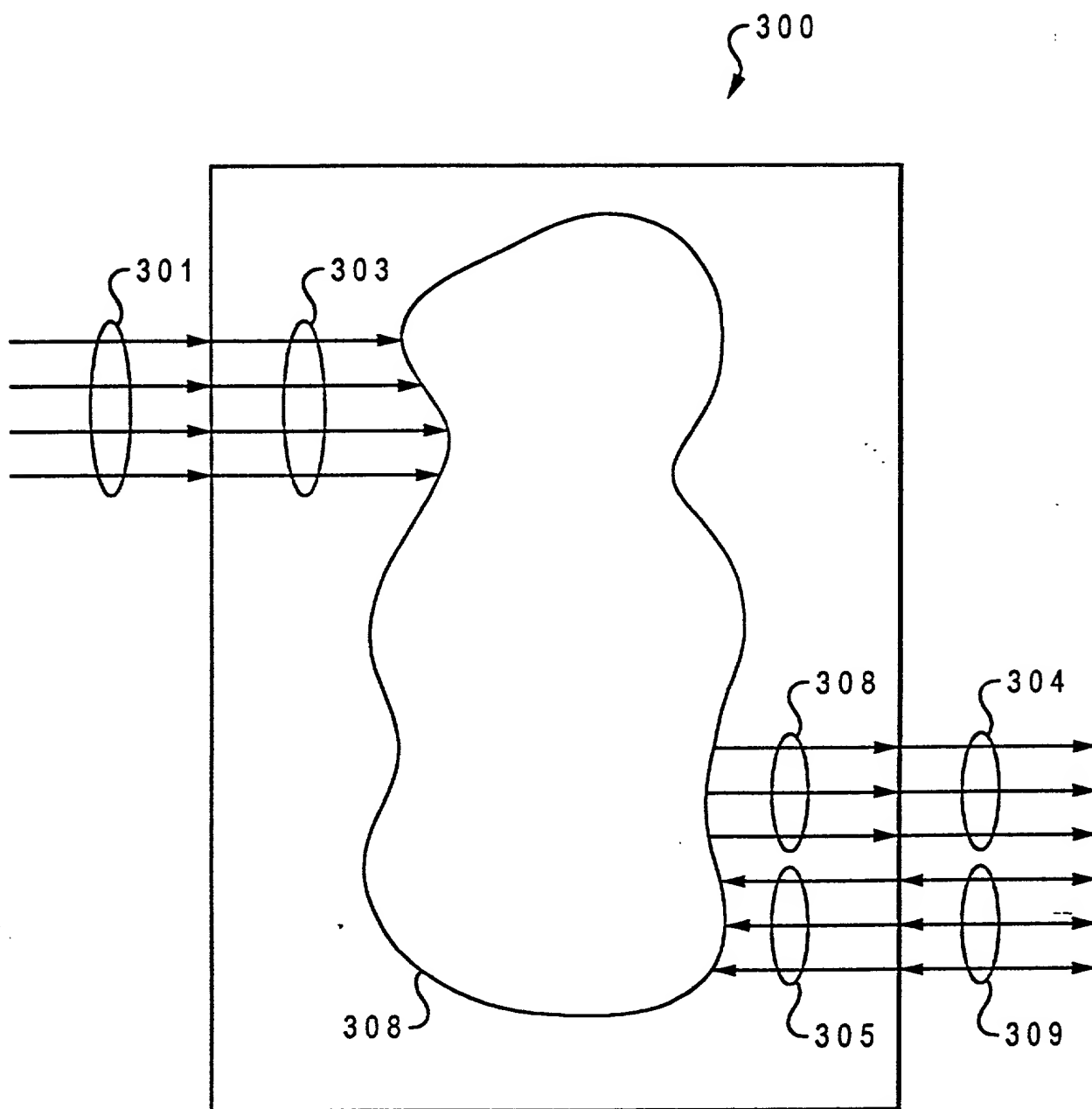


Fig. 3A

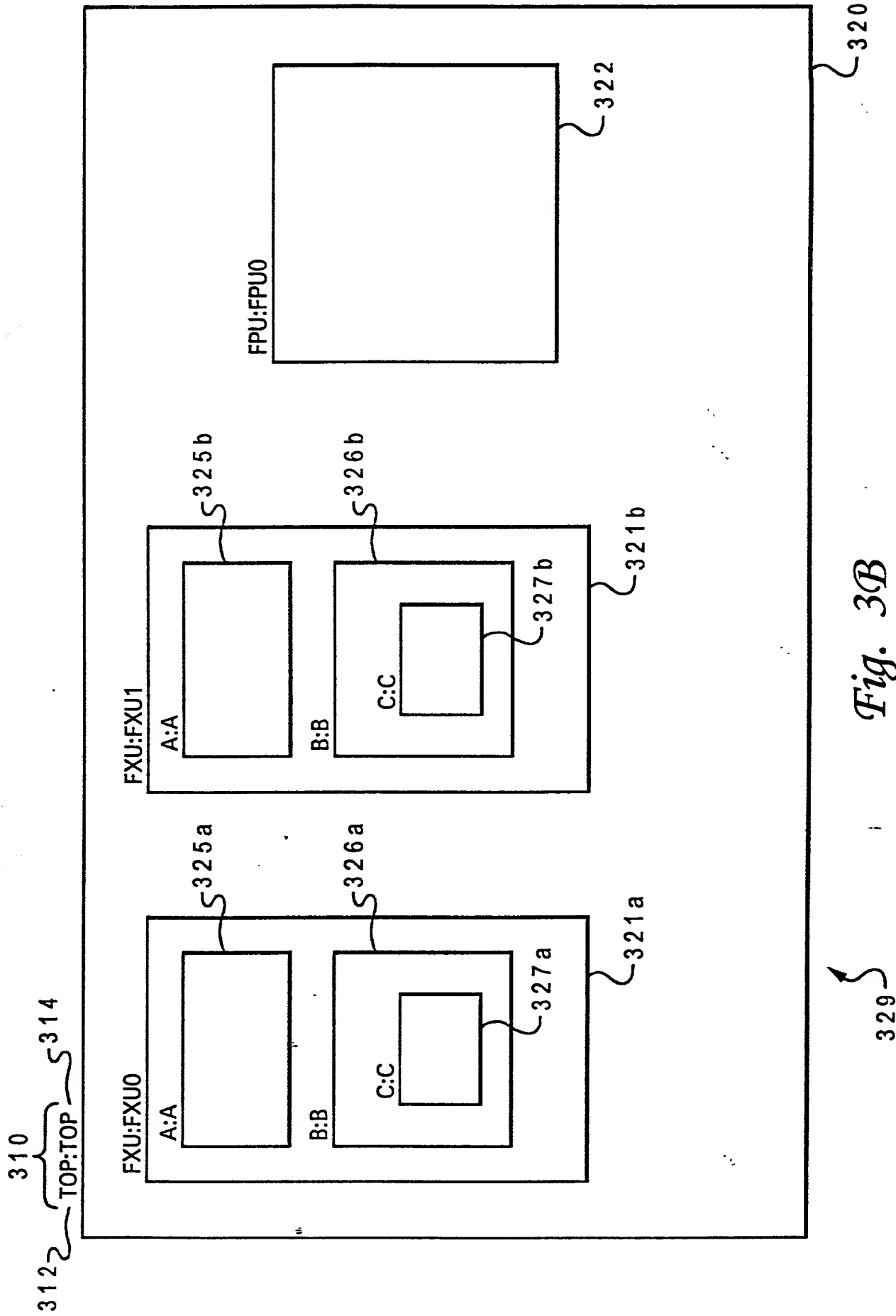


Fig. 3B

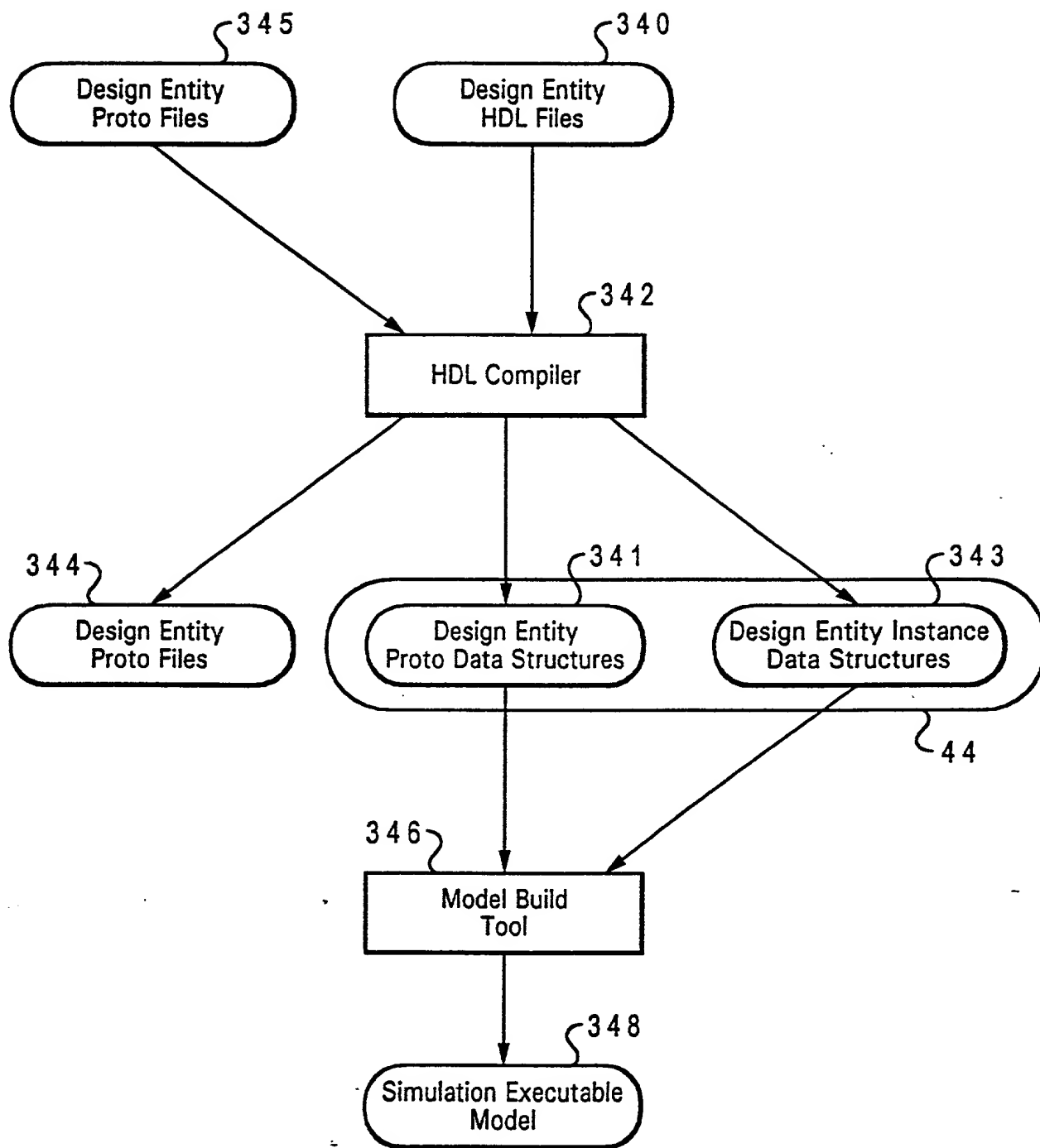


Fig. 3C

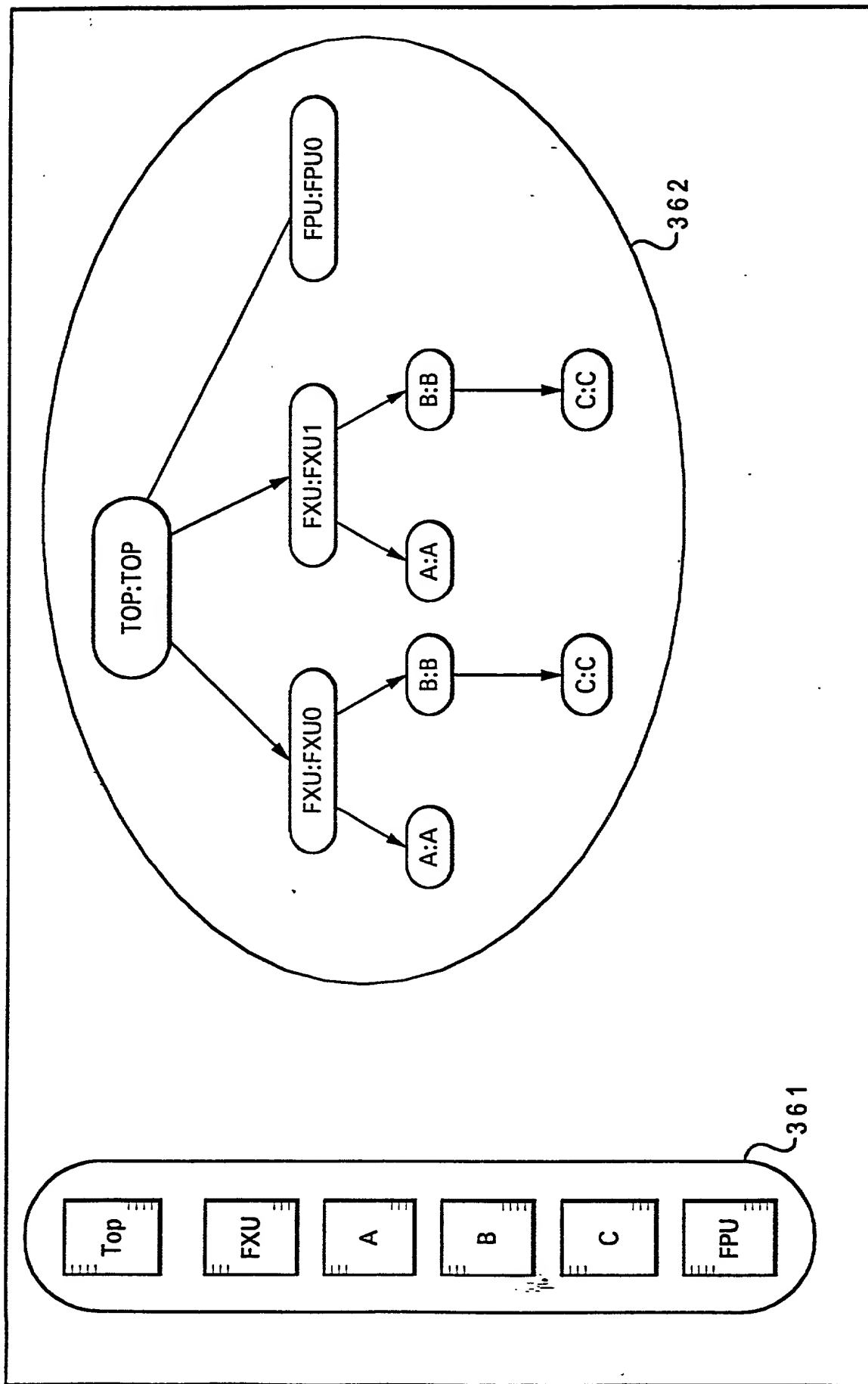


Fig. 3D

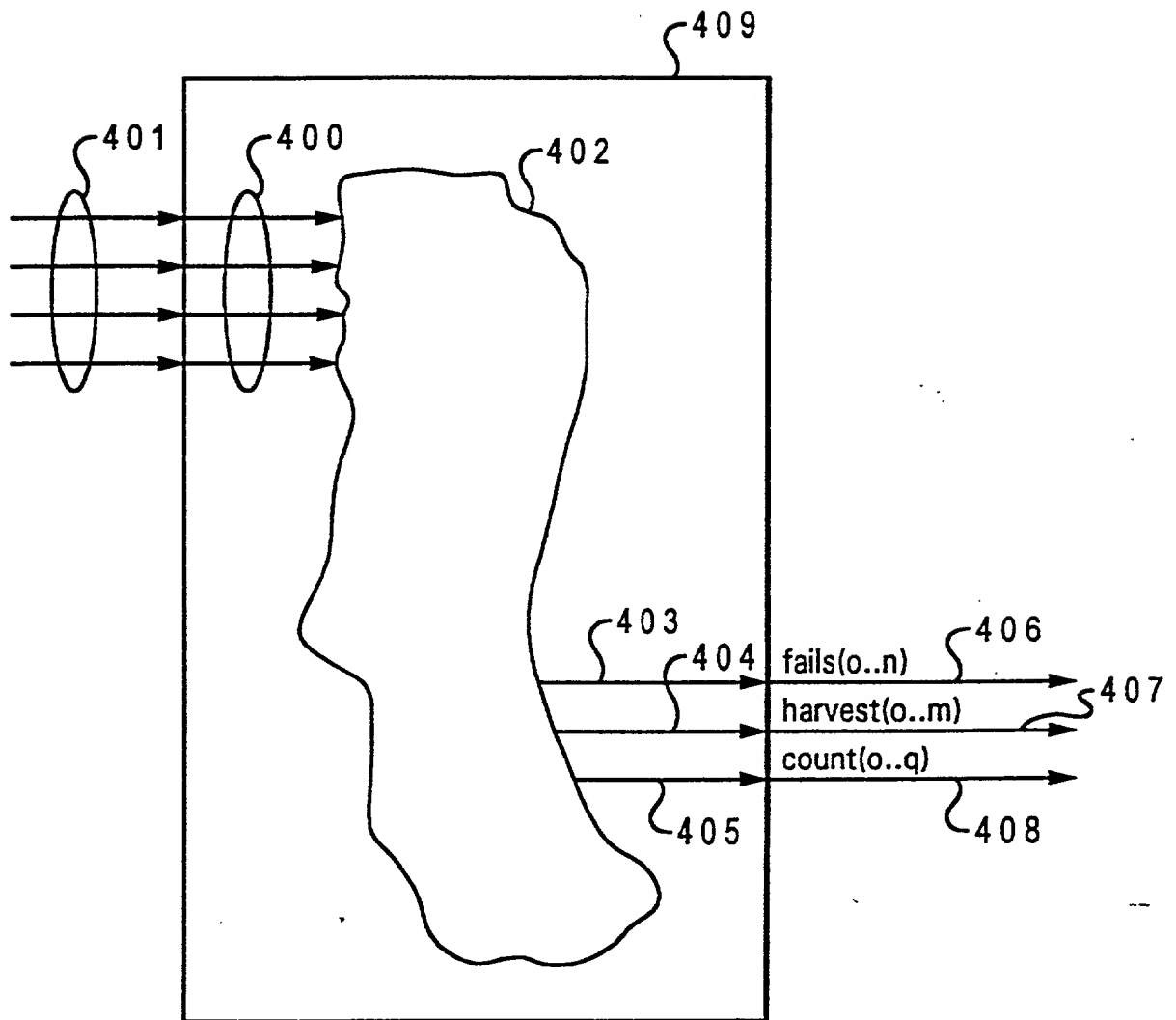


Fig. 4A

TOP:TOP

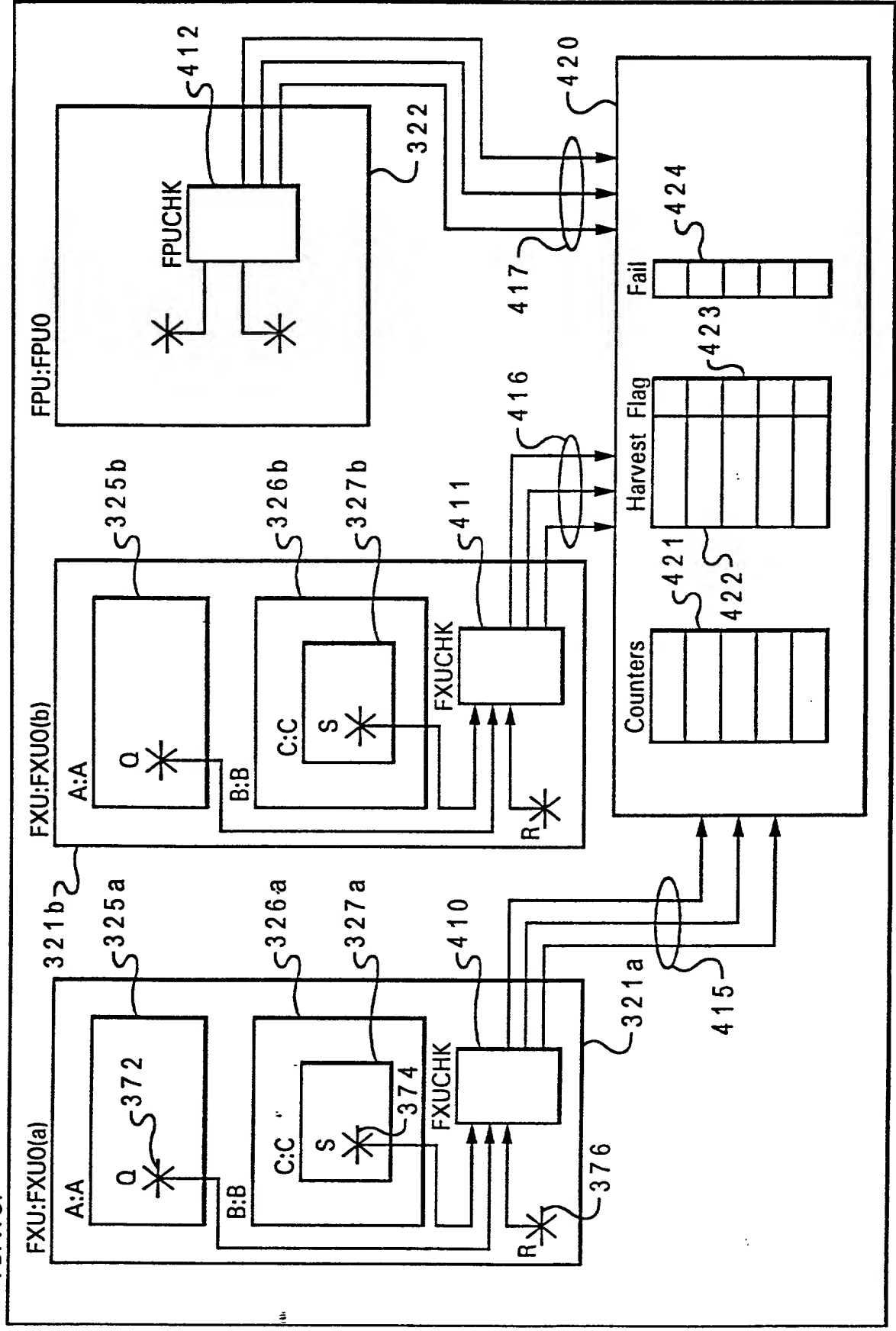


Fig. 4B

329

ENTITY FXUCHK IS

```

PORT(  S_IN      :  IN std_ulogic;
        Q_IN      :  IN std_ulogic;
        R_IN      :  IN std_ulogic;
        clock      :  IN std_ulogic;
        fails      :  OUT std_ulogic_vector(0 to 1);
        counts     :  OUT std_ulogic_vector(0 to 2);
        harvests   :  OUT std_ulogic_vector(0 to 1);
);

```

4 5 0

4 5 2 { --!! BEGIN
--!! Design Entity: FXU;

4 5 3 { --!! Inputs
--!! S_IN => B.C.S;
--!! Q_IN => A.Q;
--!! R_IN => R;
--!! CLOCK => clock;
--!! End Inputs

4 5 4 { --!! Fail Outputs;
--!! 0 : "Fail message for failure event 0";
--!! 1 : "Fail message for failure event 1";
--!! End Fail Outputs;

4 5 5 { --!! Count Outputs;
--!! 0 : <event0> clock;
--!! 1 : <event1> clock;
--!! 2 : <event2> clock;
--!! End Count Outputs;

4 5 6 { --!! Harvest Outputs;
--!! 0 : "Message for harvest event 0";
--!! 1 : "Message for harvest event 1";
--!! End Harvest Outputs;

4 5 7 { --!! End;

4 5 1

4 4 0

ARCHITECTURE example of FXUCHK IS

BEGIN

... HDL code for entity body section ...

END;

4 5 8

Fig. 4C

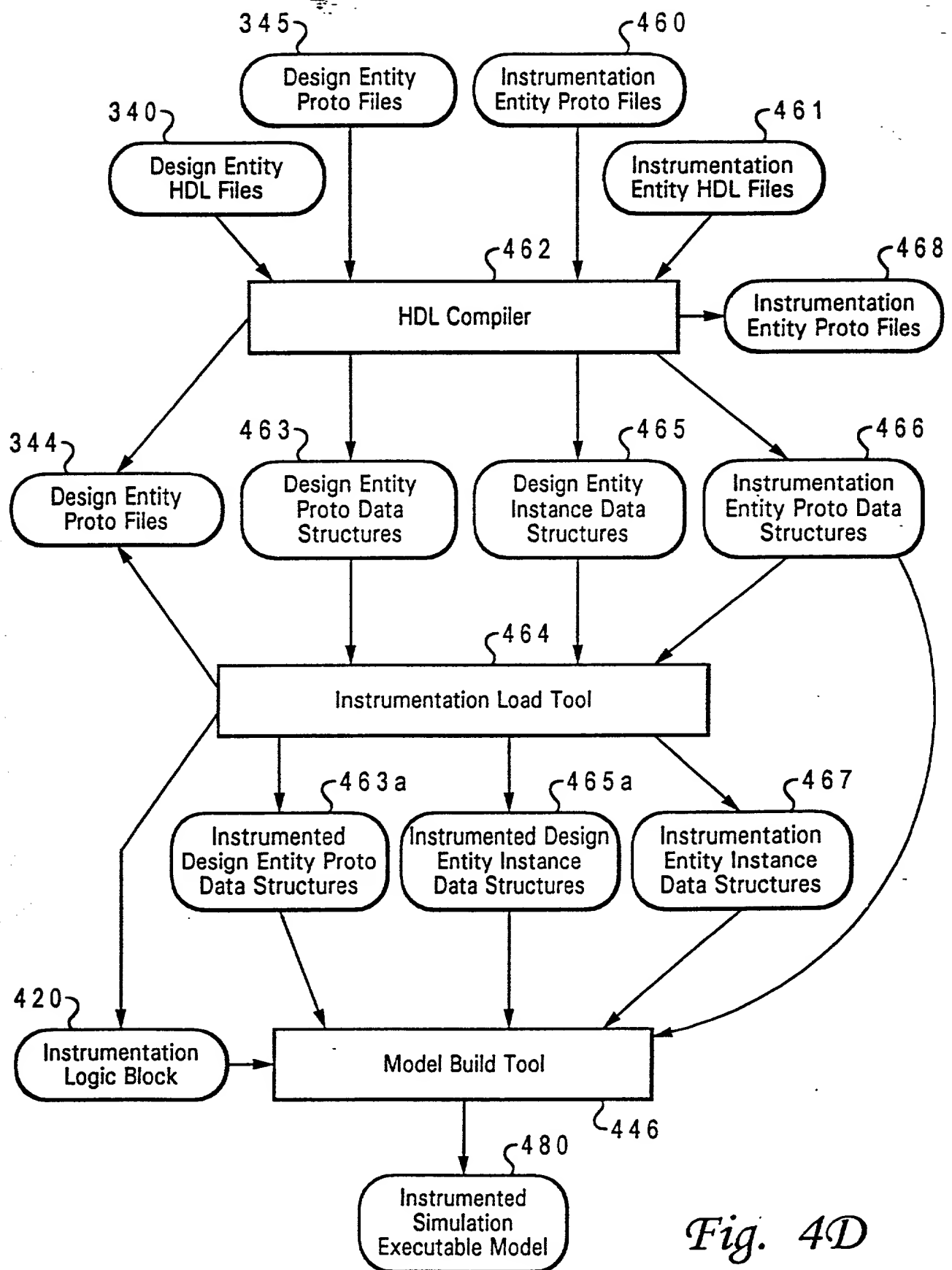


Fig. 4D

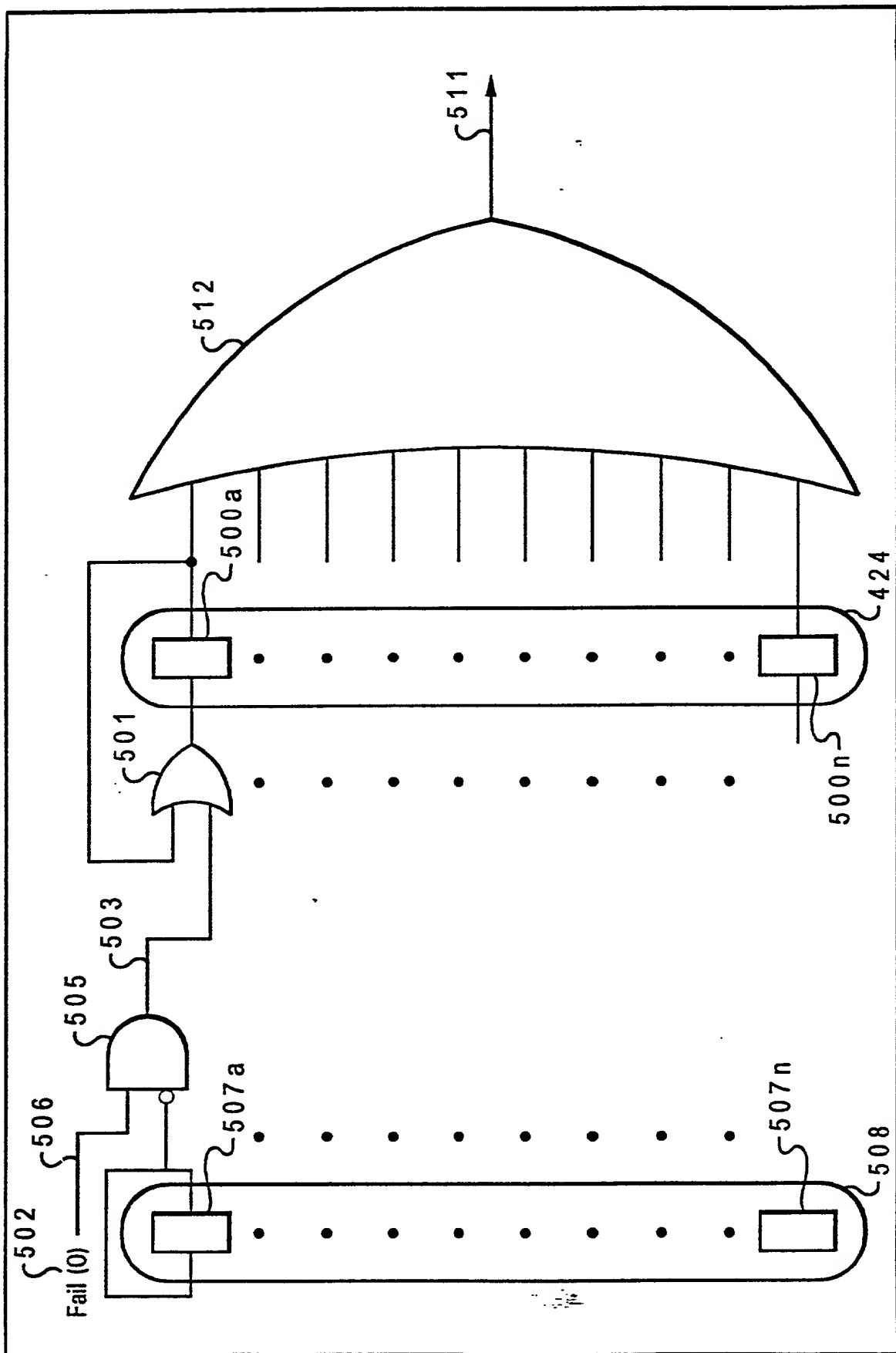


Fig. 5A

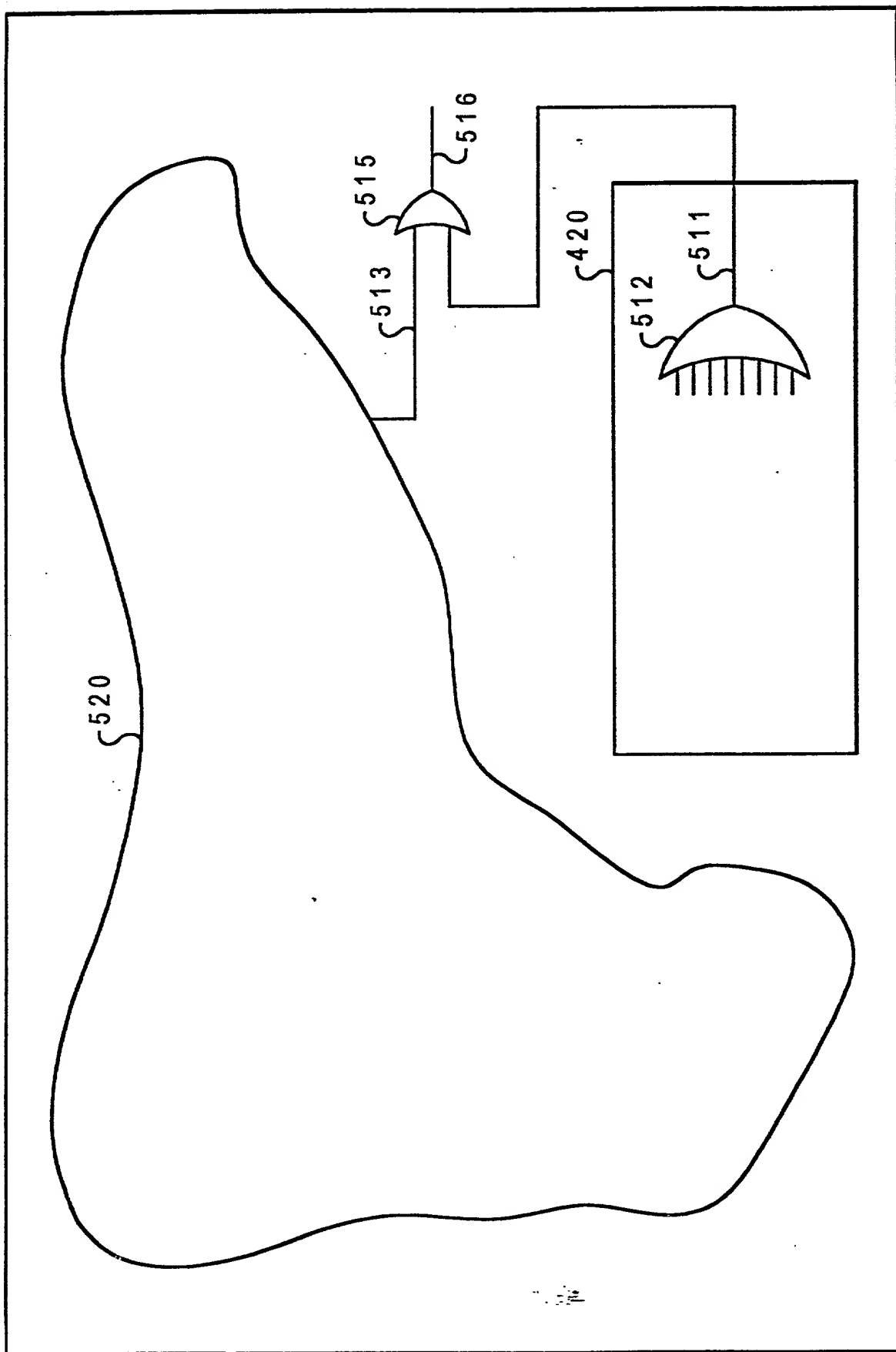


Fig. 5B

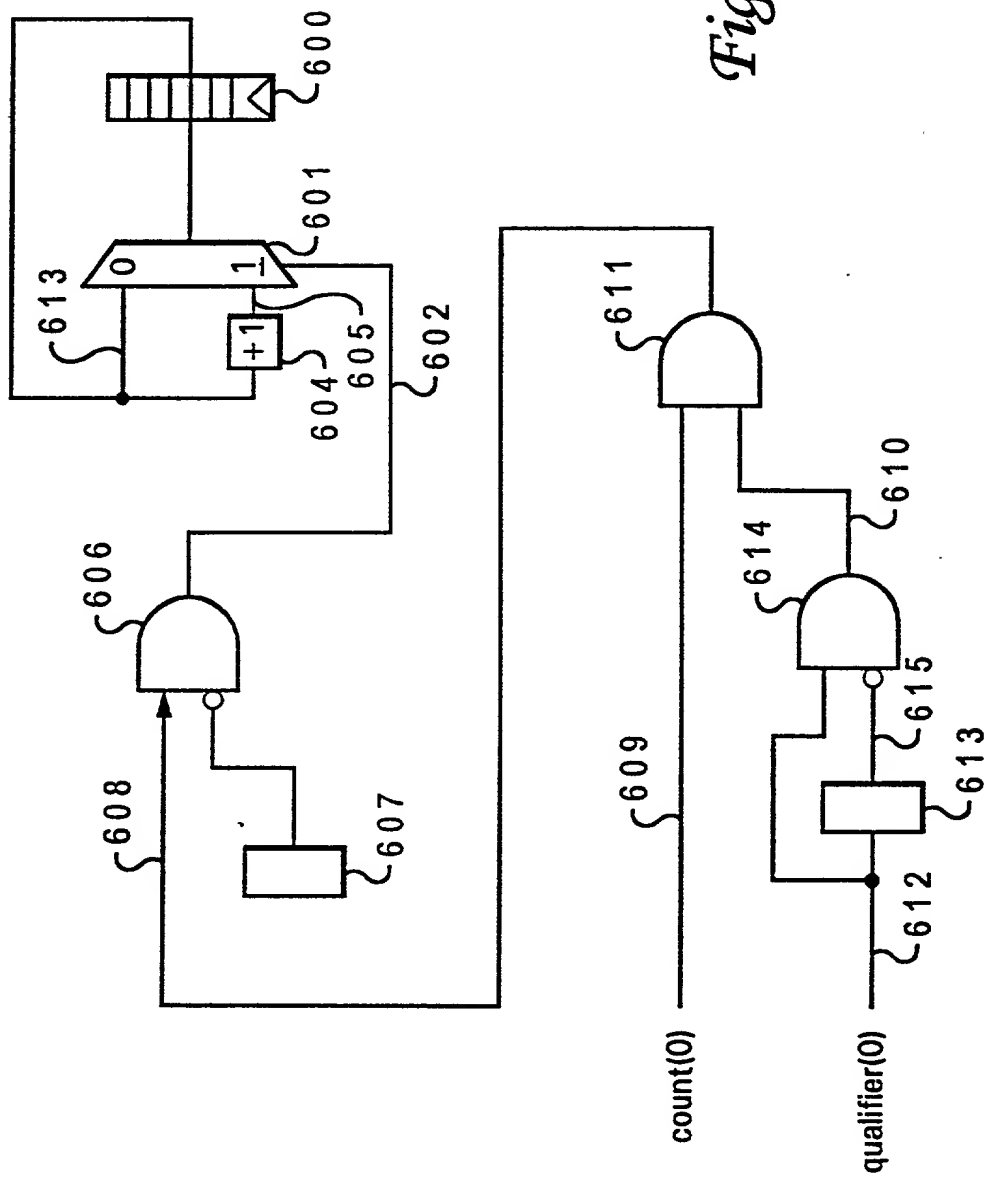


Fig. 6A

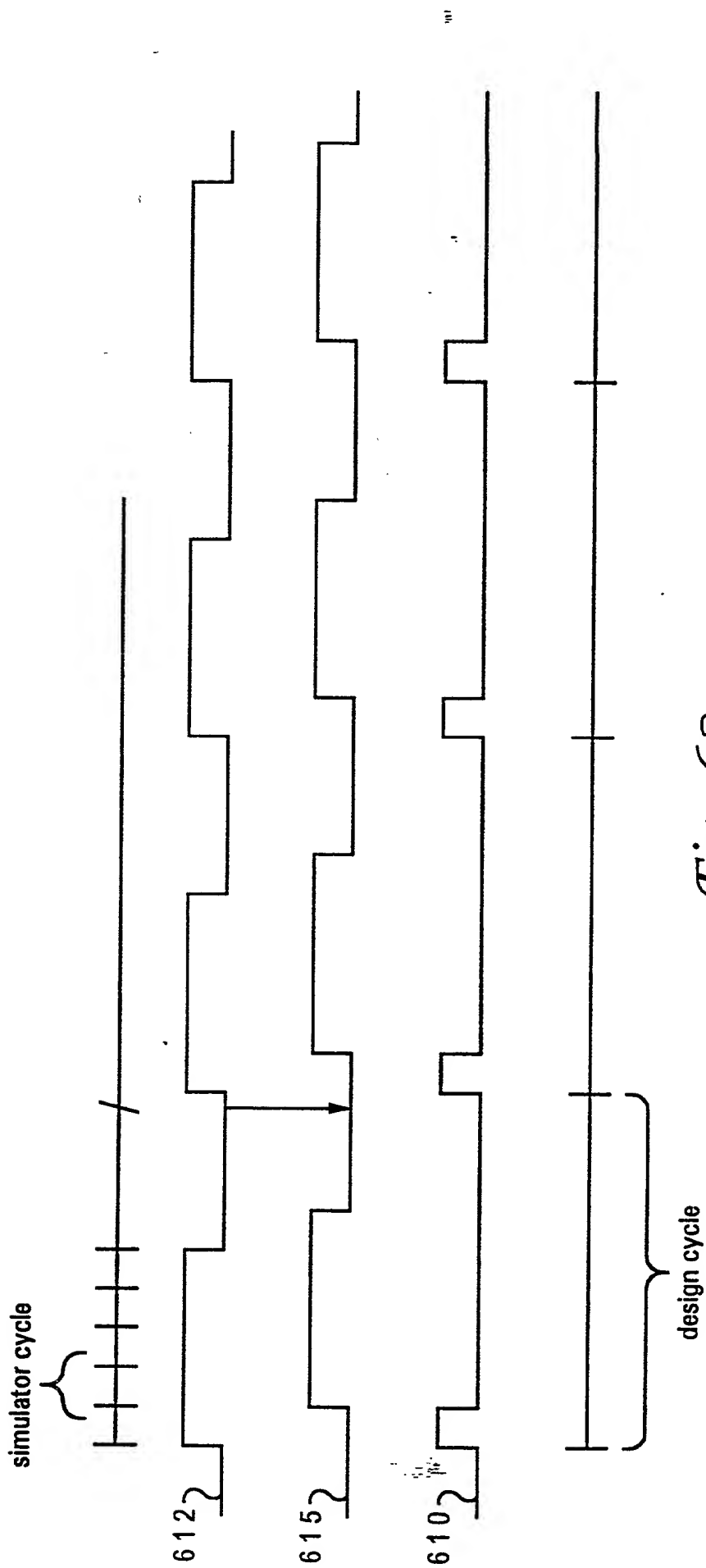


Fig. 6B

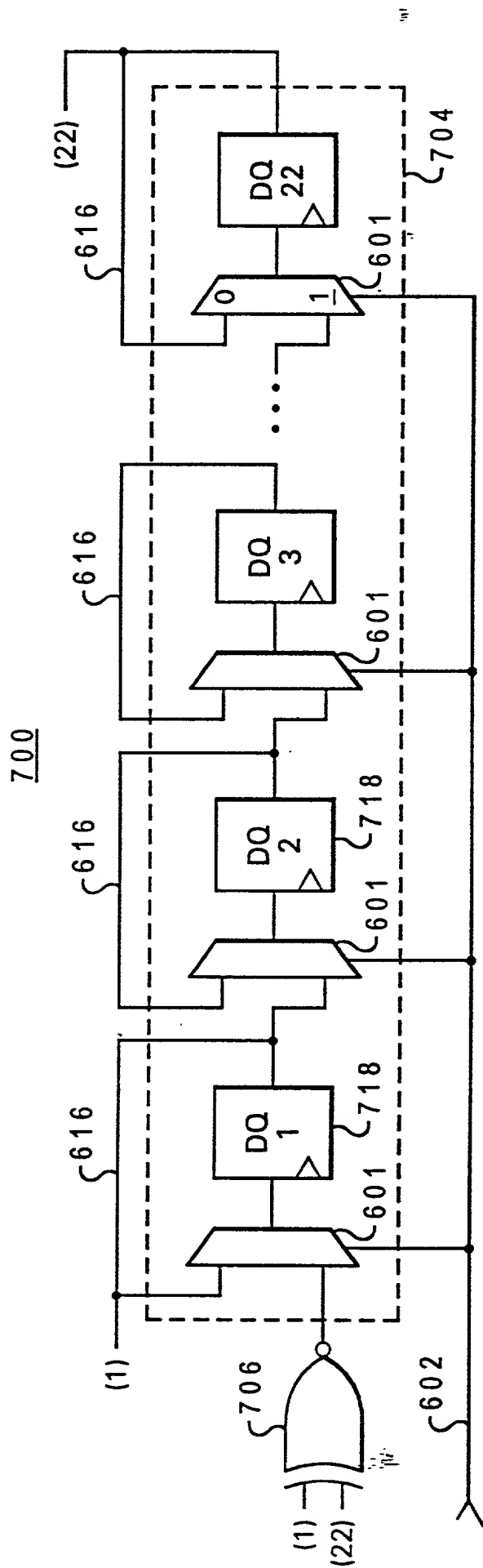


Fig. 7

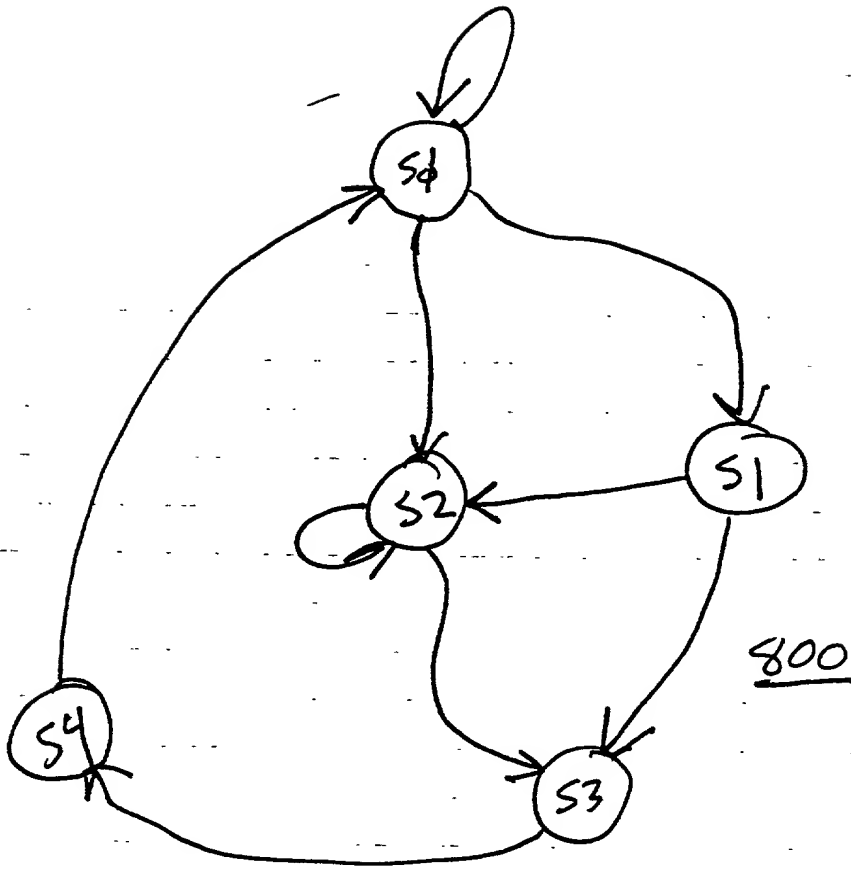


FIG. 8

(Prior Art)

entity Fsm; Fsm

850

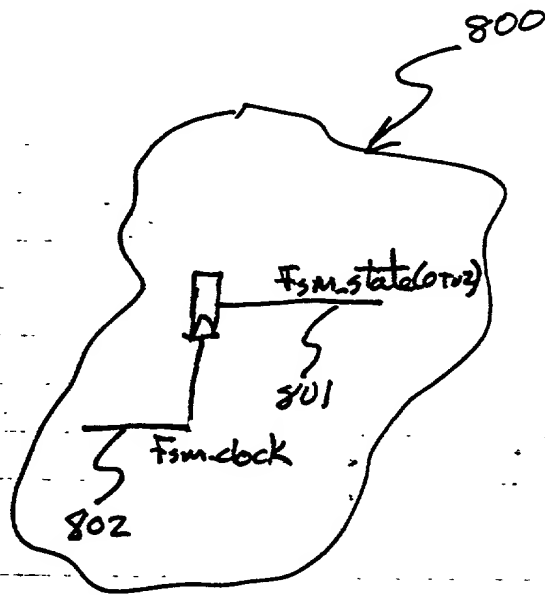


FIG. 8A
(Prior Art)

entity Fsm IS

PORT (

.... ports for entity Fsm

);

ARCHITECTURE Fsm of Fsm IS

BEGIN

.... HDL code for Fsm and rest of the entity. ...

fsm-state(0 to 2) <= ... signal 801

```
853 E --!! Embedded Fsm : exampleFsm;
859 E --!! clock : (fsm_clock);
854 E --!! state_vector : (fsm_state(0 to 2));
855 E --!! states vector : (s0, s1, s2, s3, s4);
856 E --!! state_encoding : ('000', '001', '010', '011', '100');
857 E --!! arcs : (s0 => s0, s0 => s1, s0 => s2,
               s1 => s2, s1 => s3, s2 => s2,
               s2 => s3, s3 => s4, s4 => s0);
858 E --!! end Fsm;
```

852
86

END;

FIG. 8B

Handwritten signature

entity FSM:FSM

850

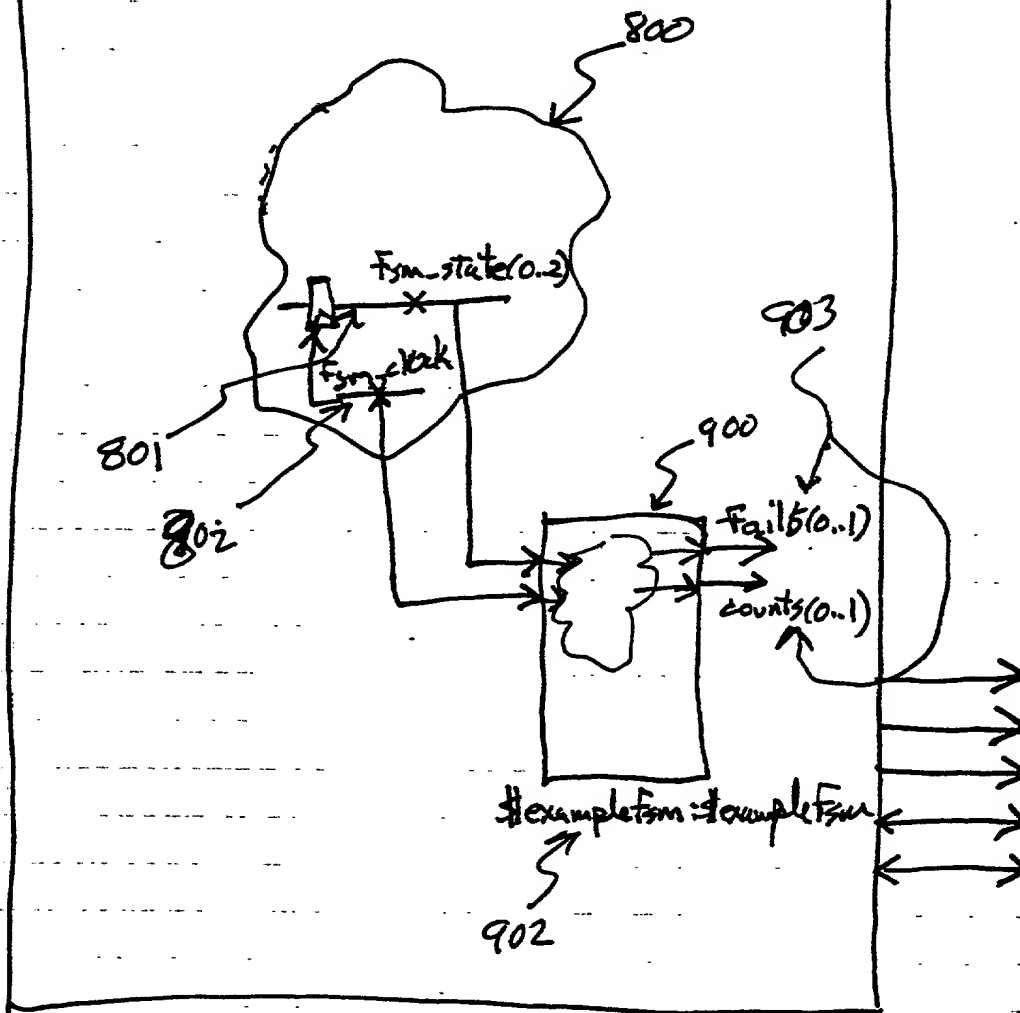


FIG. 9

TOP: TOP

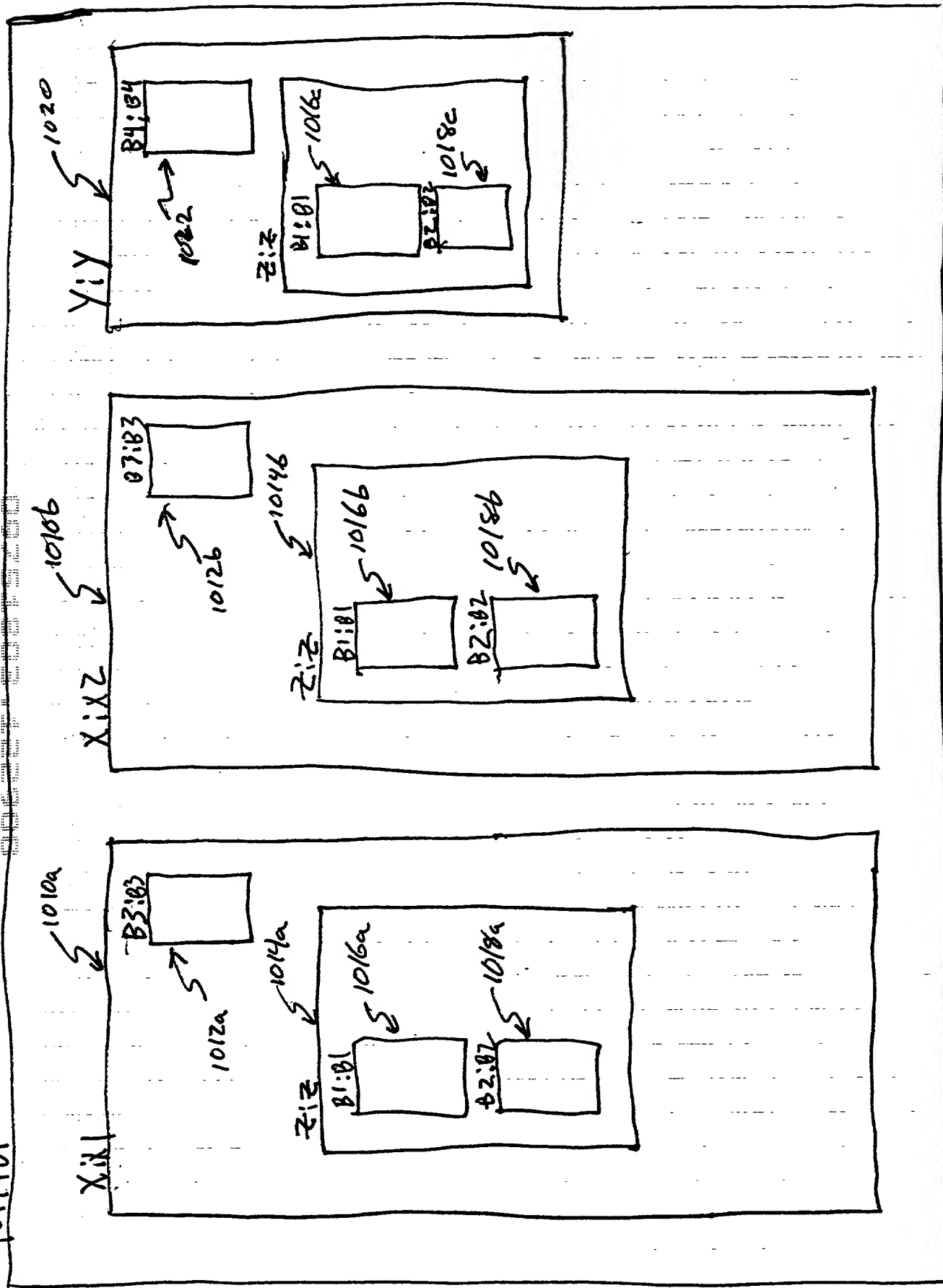


FIG. 10A

1030

1032

1034

1036

<instantiation identifier>, <instrumentation entity name>, <design entity name>, <event name>

FIG 10B

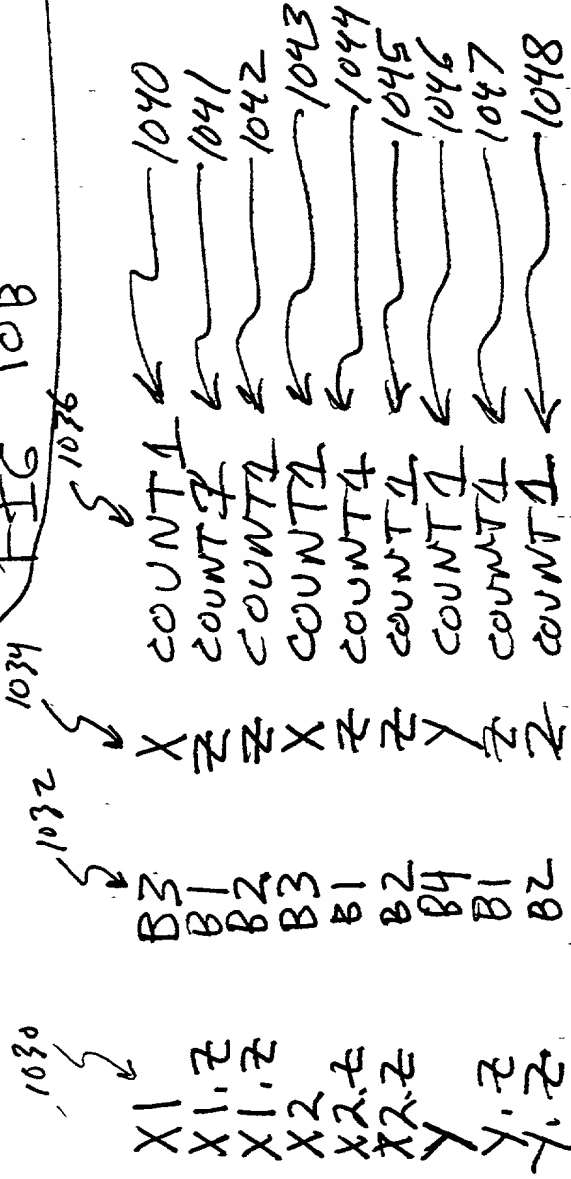


FIG 10C

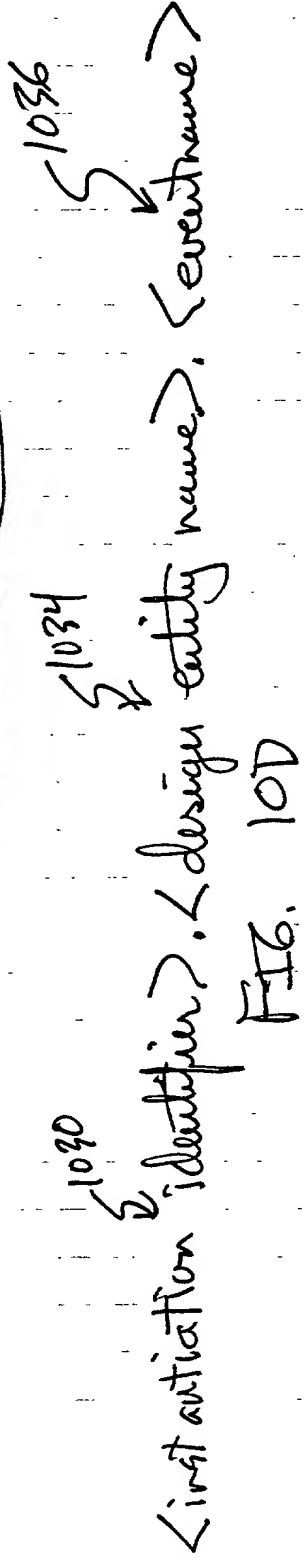
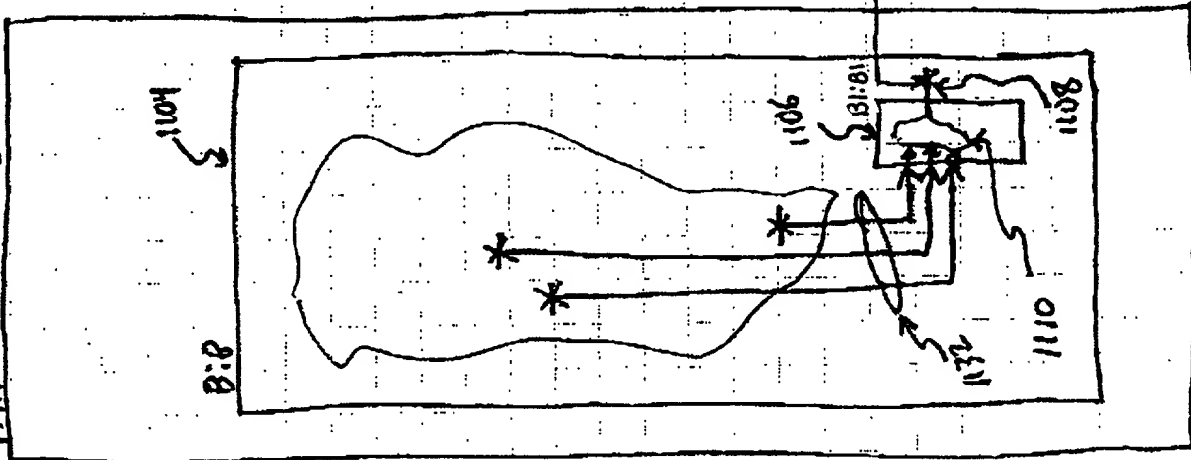


FIG. 10D

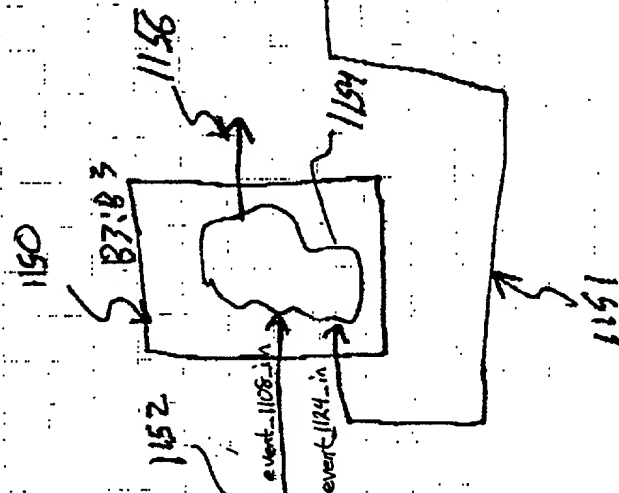
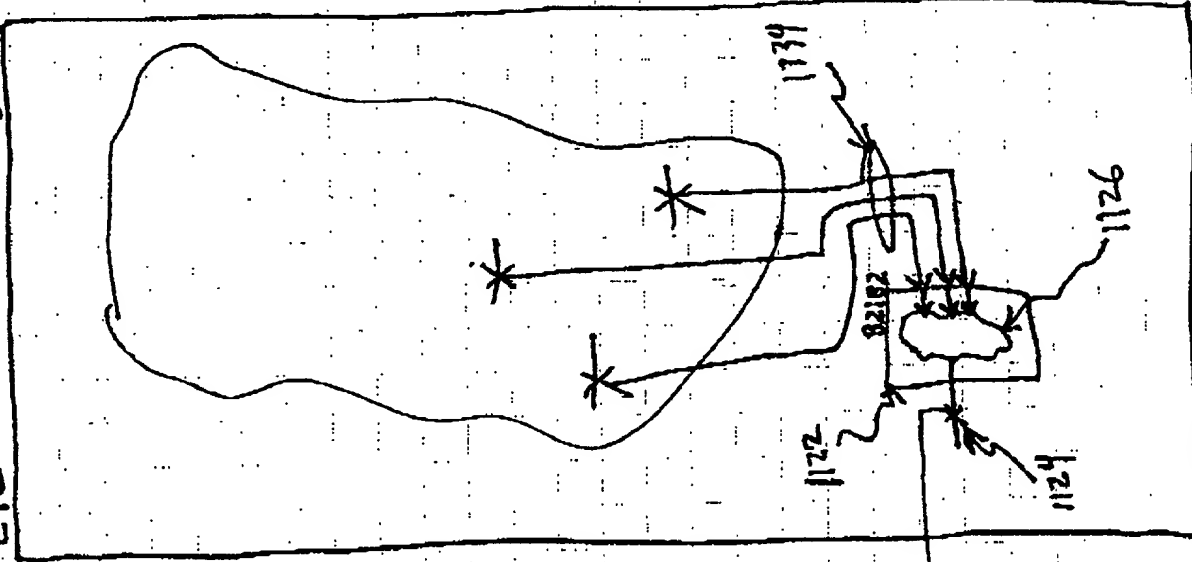
005221" E00T5259 1130

TOP:TOP

A:A 1102



C:C 11203



1100

FIG. 11A

X:X

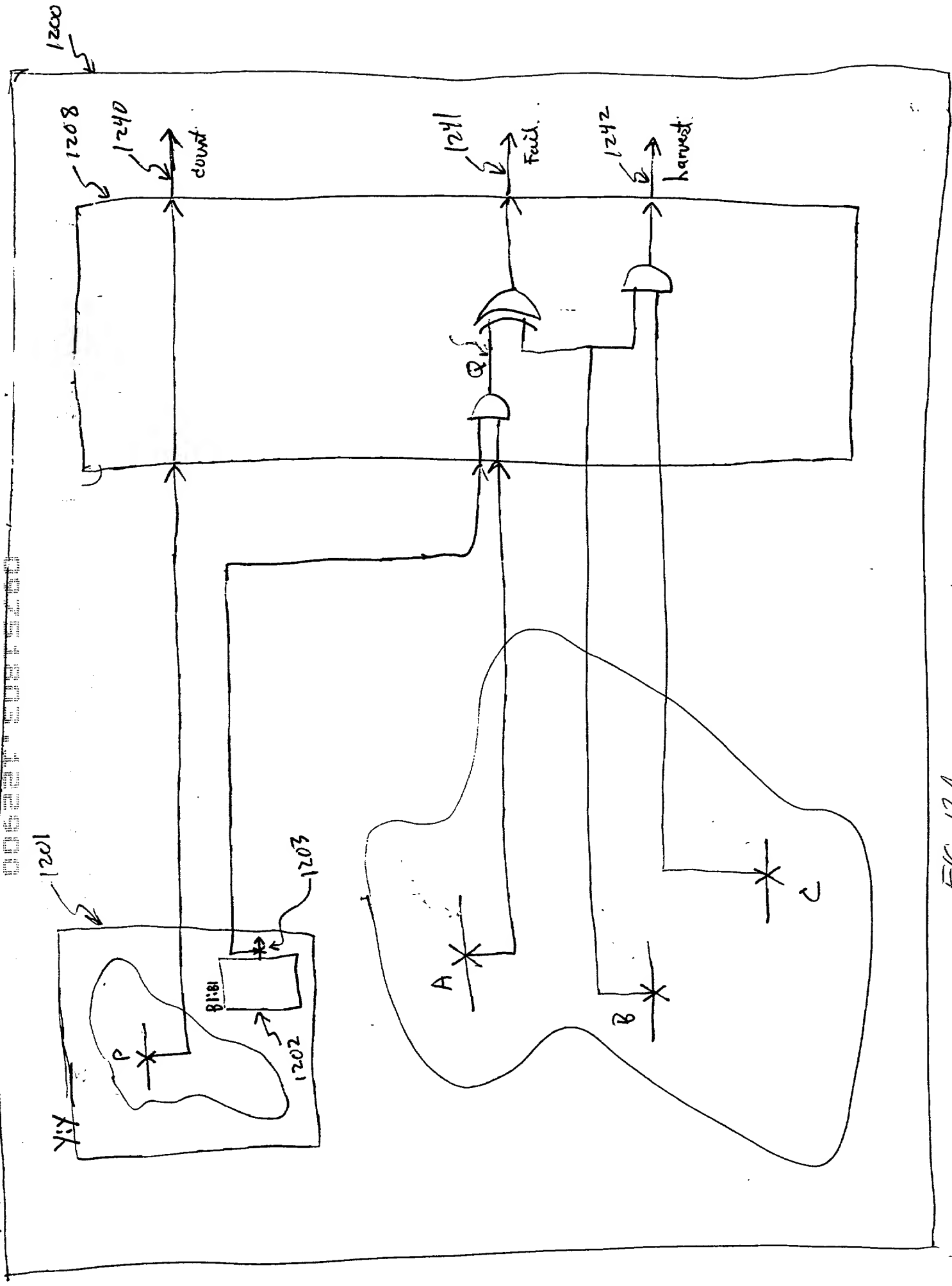


FIG. 12A

Entity X IS

PORT (
;
);

ARCHITECTURE example OF X IS

BEGIN

...HDL CODE FOR X....

Y:Y
PORT MAP(
);

1221

A <= ...
B <= ...
C <= ...

1222

--!! [count, countnameφ, clock] <= Y.P; 1230
--!! Q <= Y.[B].count.count1 AND A; 1232
--!! [fail, failnameφ, "fail msg"] <= Q XOR B; 1234
--!! [harvest, harvestnameφ, "harvest msg"] <= B AND C; 1236

END

FIG. 12B

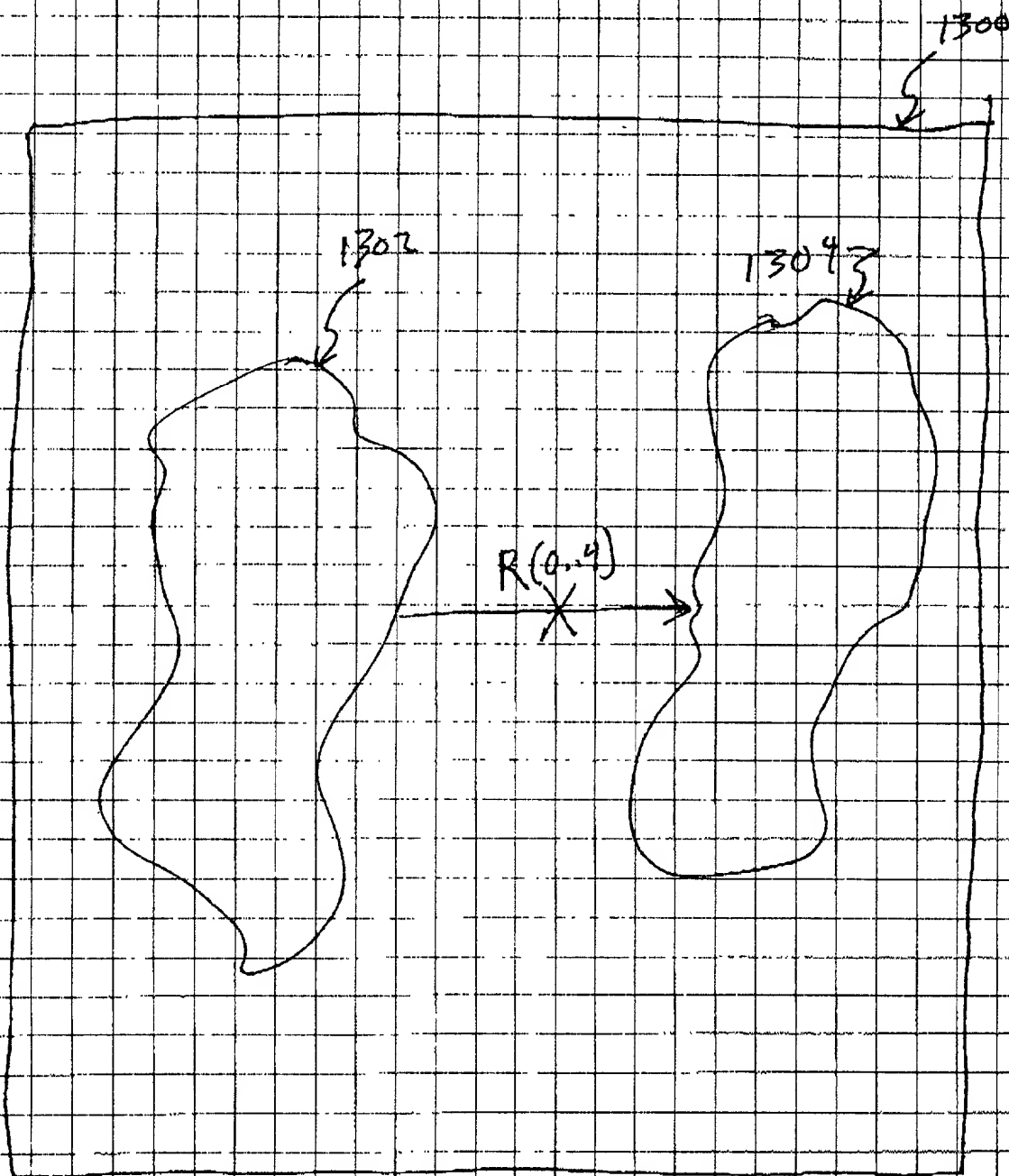


FIG. 13A

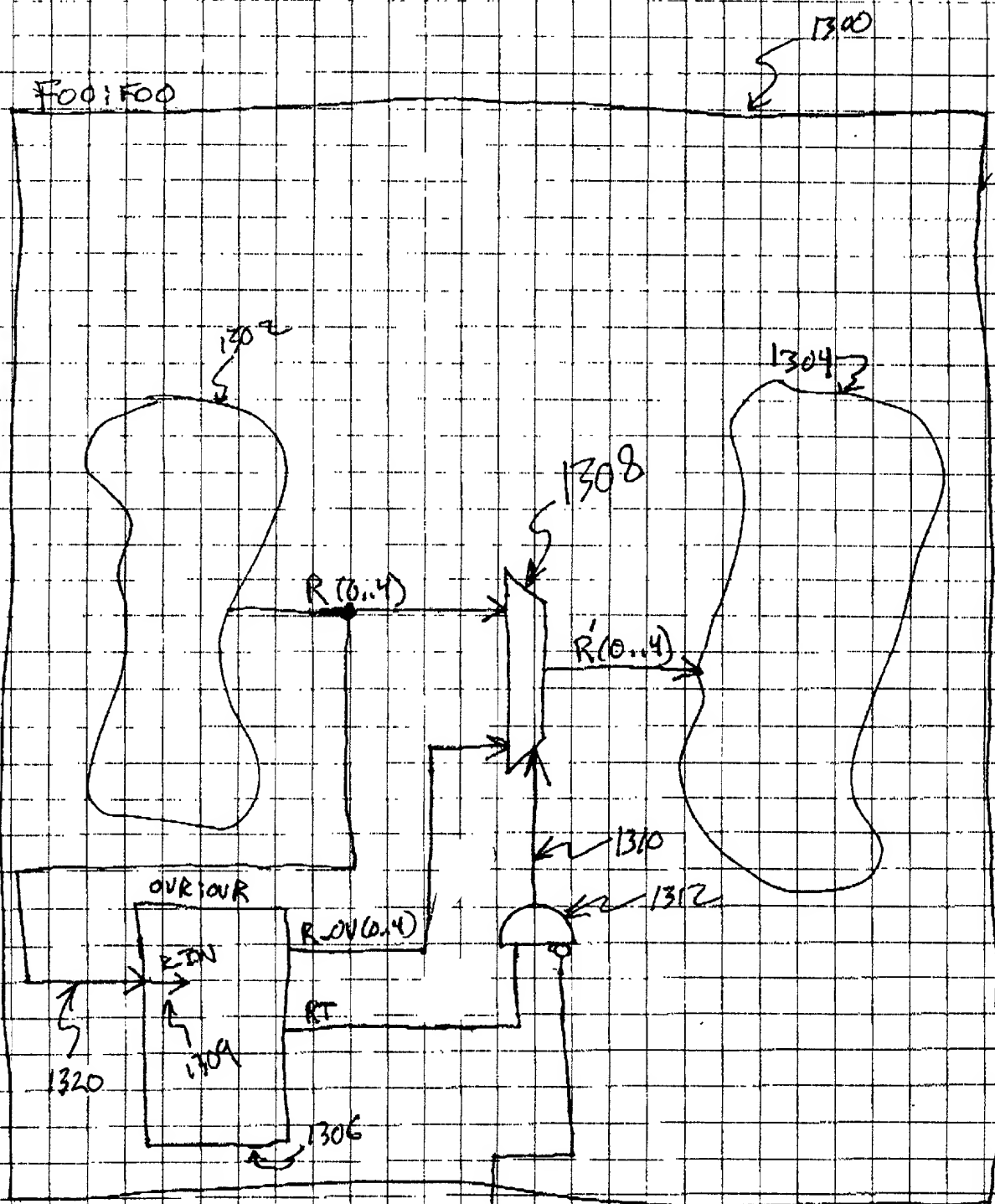
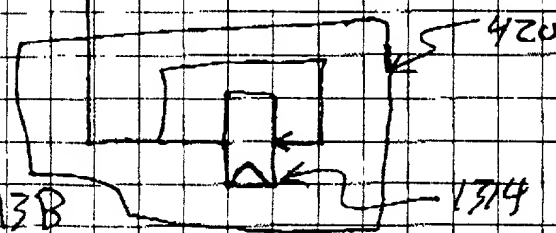


FIG. 13B



ENTITY OVR IS

PORT(R_IN : IN std_logic_vector(0..4);

-- other ports as required --

R_OV : OUT std_logic_vector(0..4);
RT : OUT std_logic

-- !! BEGIN

-- !! Design Entity: FOO;

-- !! inputs (total)
-- !! R_IN => { R(0..4) };

-- !! other ports as needed

-- !! END INPUTS

-- !! OUTPUTS

-- !! <R-OVERRIDE>: R_OV(0..4) => R(0..4) [RT];

-- !! END

ARCHITECTURE example of OVR IS

BEGIN

.... HDL code for entity body section

END

FIG. 13C

ENTITY Foo IS

PORT (
...
);

ARCHITECTURE example of Foo IS

BEGIN

...
...
...

R <= ...

...
...

1380 {
--!! R_IN <= R; 1381
--!!
--!!
--!! R_OV(0..4) <= ...; 1382
--!! RT <= ...; 1383
--!! Coverride, R_OVERRIDE, R(0..4), RT] <= R_OV(0..4);
384

FIG. 13D